AMENDMENTS TO THE CLAIMS:

Please amend the claims as follows, substituting any amended claim(s) for the corresponding pending claim(s):

1. (Currently Amended) A hot patch system ~~for changing of code in a processor~~ comprising~~;~~ ~~in combination~~:

a read only memory ~~for~~ storing a plurality of instructions;

a cache memory storing alternate instructions for at least one instruction stored within the read only memory, each cache line within the cache memory having associated therewith one or more selection flags;

a program counter coupled to the read only memory and to the cache memory, the program counter transmitting an address to both the read only memory and the cache memory ~~for indexing of the memory to access an instruction~~; and

~~a~~ cache ~~system~~ control logic coupled to the cache memory, the cache control logic ~~and to the program counter for~~ comparing selected information associated with ~~the instructions from~~ an instruction stored at the address in the read only memory with counterpart selected information associated with an instruction stored at the address in the cache ~~system and for altering an instruction stream when there is a comparison match~~ memory, wherein the selected information and counterpart selected information are selected based upon the one or more selection flags associated with a cache line corresponding to the address.

Claims 2–22 (Canceled).

Please add the following new claims:

23. (Newly Added) The hot patch system according to claim 1, wherein the one or more selection flags include a first flag indicating whether the cache control logic is to compare addresses and a second flag indicating whether the cache control logic is to compare opcodes.

24. (Newly Added) The hot patch system according to claim 23, wherein the second flag, when set, indicates that the cache control logic is to compare an opcode stored at the address within the read only memory with an opcode stored at the address within the cache memory.

25. (Newly Added) The hot patch system according to claim 23, wherein the first and second flags may be individually set, so that both flags may be set, one flag may be set while the other flag is not set, or both flags may be not set.

25. (Newly Added) The hot patch system according to claim 23, wherein the one or more selection flags further include a third flag indicating whether an opcode comparison should be performed for every instance of an opcode within the read only memory.

26. (Newly Added) The hot patch system according to claim 1, wherein each cache line within the cache memory has associated therewith one or more instruction flow control flags, wherein the cache control logic causes a change in instruction flow based upon the one or more instruction flow control flags associated with the cache line corresponding to the address when there is a comparison match between the selected information and the counterpart selected information.

27. (Newly Added) The hot patch system according to claim 26, wherein the one or more instruction flow control flags include an insert flag indicating that an opcode at the address within the cache memory is to be inserted prior to execution of an opcode at the address within the read only memory.

28. (Newly Added) The hot patch system according to claim 26, wherein the one or more instruction flow control flags include a replace flag indicating that an opcode at the address within the cache memory is to be executed instead of an opcode at the address within the read only memory.

29. (Newly Added) The hot patch system according to claim 26, wherein the one or more instruction flow control flags include a block flag indicating that more than one opcode starting at the address within the cache memory are to be executed instead of or before an opcode at the address within the read only memory.

30. (Newly Added) The hot patch system according to claim 26, wherein the one or more instruction flow control flags include a noop flag indicating that an opcode at the address within the read only memory is to be skipped.

31. (Newly Added) A hot patch method comprising:

storing a plurality of instructions within a read only memory;

storing alternate instructions for at least one instruction in the read only memory within a cache memory, each cache line within the cache memory having associated therewith one or more selection flags;

transmitting an address to both the read only memory and the cache memory; and

comparing selected information associated with an instruction stored at the address in the read only memory with counterpart selected information associated with an instruction stored at the address in the cache memory, wherein the selected information and counterpart selected information are selected based upon the one or more selection flags associated with a cache line corresponding to the address.

32. (Newly Added) The hot patch method according to claim 31, wherein the one or more selection flags include a first flag indicating whether addresses are to be compared and a second flag indicating whether opcodes are to be compared.

33. (Newly Added) The hot patch method according to claim 32, wherein the second flag, when set, indicates that an opcode stored at the address within the read only memory is to be compared with an opcode stored at the address within the cache memory.

34. (Newly Added) The hot patch method according to claim 32, wherein the first and second flags may be individually set, so that either both flags may be set, one flag may be set while the other flag is not set, or both flags may be not set.

35. (Newly Added) The hot patch method according to claim 32, wherein the one or more selection flags further include a third flag indicating whether an opcode comparison should be performed for every instance of an opcode within the read only memory.

36. (Newly Added) The hot patch method according to claim 31, wherein each cache line within the cache memory has associated therewith one or more instruction flow control flags, wherein instruction flow is changed based upon the one or more instruction flow control flags associated with a cache line corresponding to the address when there is a comparison match between the selected information and the counterpart selected information.

37. (Newly Added) The hot patch method according to claim 36, wherein the one or more instruction flow control flags include an insert flag indicating that an opcode at the address within the cache memory is to be inserted prior to execution of an opcode at the address within the read only memory.

38. (Newly Added) The hot patch method according to claim 36, wherein the one or more instruction flow control flags include a replace flag indicating that an opcode at the address within the cache memory is to be executed instead of an opcode at the address within the read only memory.

39. (Newly Added) The hot patch method according to claim 36, wherein the one or more instruction flow control flags include a block flag indicating that more than one opcode starting at the address within the cache memory are to be executed instead of or before an opcode at the address within the read only memory.

40. (Newly Added) The hot patch method according to claim 36, wherein the one or more instruction flow control flags include a noop flag indicating that an opcode at the address within the read only memory is to be skipped.

41. (Newly Added) A hot patch system comprising:

a read only memory storing a plurality of instructions;

a cache memory storing alternate instructions for at least one instruction stored within the read only memory, each cache line within the cache memory having associated therewith one or more selection flags and one or more instruction flow control flags; and

cache control logic coupled to the cache memory, the cache control logic comparing selected information associated with an instruction stored at a specified address in the read only memory with counterpart selected information associated with an instruction stored at the specified address in the cache memory,

wherein the selected information and counterpart selected information are selected based upon the one or more selection flags associated with a cache line corresponding to the specified address, and

wherein the cache control logic causes a change in instruction flow based upon the one or more instruction flow control flags associated with the cache line corresponding to the address when there is a comparison match between the selected information and the counterpart selected information.

42. (Newly Added) The hot patch system according to claim 41, wherein the one or more selection flags include:

a first flag indicating whether the cache control logic is to compare the specified address with an address of one or more instructions within the cache memory;

a second flag indicating whether the cache control logic is to compare an opcode stored at least at the specified address within the read only memory with an opcode stored at the specified address within the cache memory; and

a third flag indicating whether the cache control logic is to compare an opcode stored at any address within the read only memory with an opcode stored at the specified address within the cache memory.

43. (Newly Added) The hot patch system according to claim 41, wherein the one or more instruction flow control flags include:

a replace flag indicating that an opcode at the specified address within the cache memory is to be executed instead of an opcode at the specified address within the read only memory;

a block flag indicating that more than one opcodes starting at the specified address within the cache memory are to be executed instead of or before an opcode at the specified address within the read only memory; and

a noop flag indicating that an opcode at the specified address within the read only memory is to be skipped.